Notice of Allowability	Application No.	Applicant(s)	
	09/978,475	ROSE ET AL.	
	Examiner	Art Unit	
	KAREN TANG	2447	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Appeal filed on 10/3/2011*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-4,6-8,10-12,14-16,24-27,30-32,34,35,37 and 38*.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20111109* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Karen C Tang/
Primary Examiner, Art Unit 2447

EXAMINER'S AMENDMENT

1) An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2) Authorization for this examiner's amendment was given in a telephone interview with Eric Stephenson, Reg. No. 38,321 on November 8th, 2011.

3) The application is amended as follows:

Amendments to the Claims:

1. (**Currently Amendment**) A method comprising:

receiving data from a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time;

generating a first data quantity value representing a quantity of data stored in the memory at a first point in time,

comparing the first data quantity value to a first predetermined value;

causing the transmitting device to transmit data at a second non-zero rate to the memory for storage therein during a second period of time, in response to the comparing;

modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value;

wherein the second period of time is subsequent to the first period of time; and wherein the second non-zero rate is greater than the first non-zero rate;

wherein the modifying the first predetermined value comprises subtracting a set value from the first predetermined value thereby generating a new first predetermined value.

2. (Previously Presented) The method of claim 1 wherein the memory device comprises a FIFO buffer.

3. (Original) The method of claim 1 wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

4. (Previously Presented) The method of claim 1 further comprising:

generating a rate control signal; and

transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate;

wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

5. (Cancelled)

6. (Previously Presented) The method of claim 4 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

7. (Previously Presented) The method of claim 4 further comprising:

generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

comparing the first data quantity value to the second data quantity value;

wherein the rate control signal is generated only if the first data quantity value is not equal to the second data quantity value.

8. (Previously Presented) The method of claim 1 wherein generating the first data quantity value comprises:

generating total data input count at the first point in time, wherein the total data input count represents a quantity of data input to the memory device during a period of time ending in the first point in time;

generating total data output count at the first point in time, wherein the total data output count represents a quantity of data output from the memory device during the period of time ending in the first point in time;

subtracting the total data output count from total data input count.

9. (Cancelled)

10. (**Currently Amendment**) An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a first circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate;

a second circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time;

a first comparing circuit for comparing the first data quantity value to a first predetermined value, wherein the first circuit generates the rate control signal in response to the comparing; and

a circuit for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value**;**

wherein the modifying the first predetermined value comprises subtracting a set value from the first predetermined value thereby generating a new first predetermined value.

11. (Original) The apparatus of claim 10 wherein the memory device comprises a FIFO buffer.

12. (Original) The apparatus of claim 10 further comprising the transmitting device, wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

13. (Cancelled)

14. (Previously Presented) The apparatus of claim 10 further comprising:

a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined values, wherein the first comparing circuit is one of the plurality of comparing circuits, and wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the first circuit generates the rate control signal in response to comparing the first data quantity value to the plurality of predetermined values.

15. (Previously Presented) The apparatus of claim 10 further comprising:

a third circuit for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

a second comparing circuit for comparing the first data quantity value to the second data quantity value;

wherein the first circuit generates the rate control signal only if the first data quantity value is not equal to the second data quantity value.

16. (Original) The apparatus of claim 15 wherein the first and second circuits are the same circuits.

17. – 23 (Cancelled)

24. (**Currently Amendment**) An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a first means for generating and transmitting a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate;

a second means for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time; a third means for comparing the first data quantity value to a first predetermined value; and

a means for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value;

wherein the first means generates the rate control signal in response to the comparing**;**

wherein the modifying the first predetermined value comprises subtracting a set value from the first predetermined value thereby generating a new first predetermined value.

25. (Original) The apparatus of claim 24 wherein the memory device comprises a FIFO buffer.

26. (Original) The apparatus of claim 24 further comprising the transmitting device, wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

27. (Previously Presented) The apparatus of claim 24 further comprising:

a fourth means for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

a fifth means for comparing the first data quantity value to the second data quantity value;

wherein the first means generates the rate control signal only if the first data quantity value is not equal to the second data quantity value.

28. (Cancelled)

29. (Cancelled)

30. (**Currently Amendment**) A method comprising:

receiving data from a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time;

generating a rate control signal by

generating a first data quantity value representing a quantity of data stored in the memory at a first point in time,

comparing the first data quantity value to a first predetermined value, wherein the rate control signal is generated in response to the comparing;

causing the transmitting device to transmit data at a second non-zero rate to the memory for storage therein during a second period of time, wherein

the causing comprises transmitting the rate control signal to the transmitting device; and

modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value;

wherein the second period of time is subsequent to the first period of time; and

wherein the second non-zero rate is less than the first non-zero rate**;**

wherein the modifying the first predetermined value comprises subtracting a set value from the first predetermined value thereby generating a new first predetermined value.

31. (**Currently Amendment**) An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a first circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate, wherein the second non-zero rate is less than the first non-zero rate;

a second circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time;

a first comparing circuit for comparing the first data quantity value to a first predetermined value, wherein the first circuit generates the rate control signal in response to the comparing; and

a circuit for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value**;**

wherein the modifying the first predetermined value comprises subtracting a set value from the first predetermined value thereby generating a new first predetermined value.

32. (Previously Presented) The method of claim 30 further comprising:

transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate; and

wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

33. (Cancelled)

34. (Previously Presented) The method of claim 32 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

35. (Previously Presented) The method of claim 1 wherein the causing comprises:

transmitting a rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate, wherein

the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

36. (Cancelled)

37. (Previously Presented) The method of claim 35 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

38. (Previously Presented) The method of claim 1 further comprising

the transmitting device transmitting data at a third non-zero rate to the memory for storage therein during a third period of time;

wherein the third period of time is subsequent to the second period of time, and wherein the third non-zero rate is greater than the second non-zero rate.

39-48. (Cancelled)

Reason for Allowance

The following is an examiner's statement of reasons for allowance:

None of the prior art of records teach or suggest in combination features as stated in the Examiner's Amendment Section. None of the prior art of records teach or suggest the features stated in the Examiner's Amendment Section in combination with independent claims.

While the Examiner has thoroughly reviewed the claims and has not located any errors, Applicant is encouraged to independently verify that the claims contain no typographical errors and that all claim terms have proper antecedent basis.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAREN C. TANG whose telephone number is (571)272-3116. The examiner can normally be reached on M-F 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JOON H. HWANG can be reached on (571)272-4036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Karen C Tang/
Primary Examiner, Art Unit 2447